

COVER PAGE

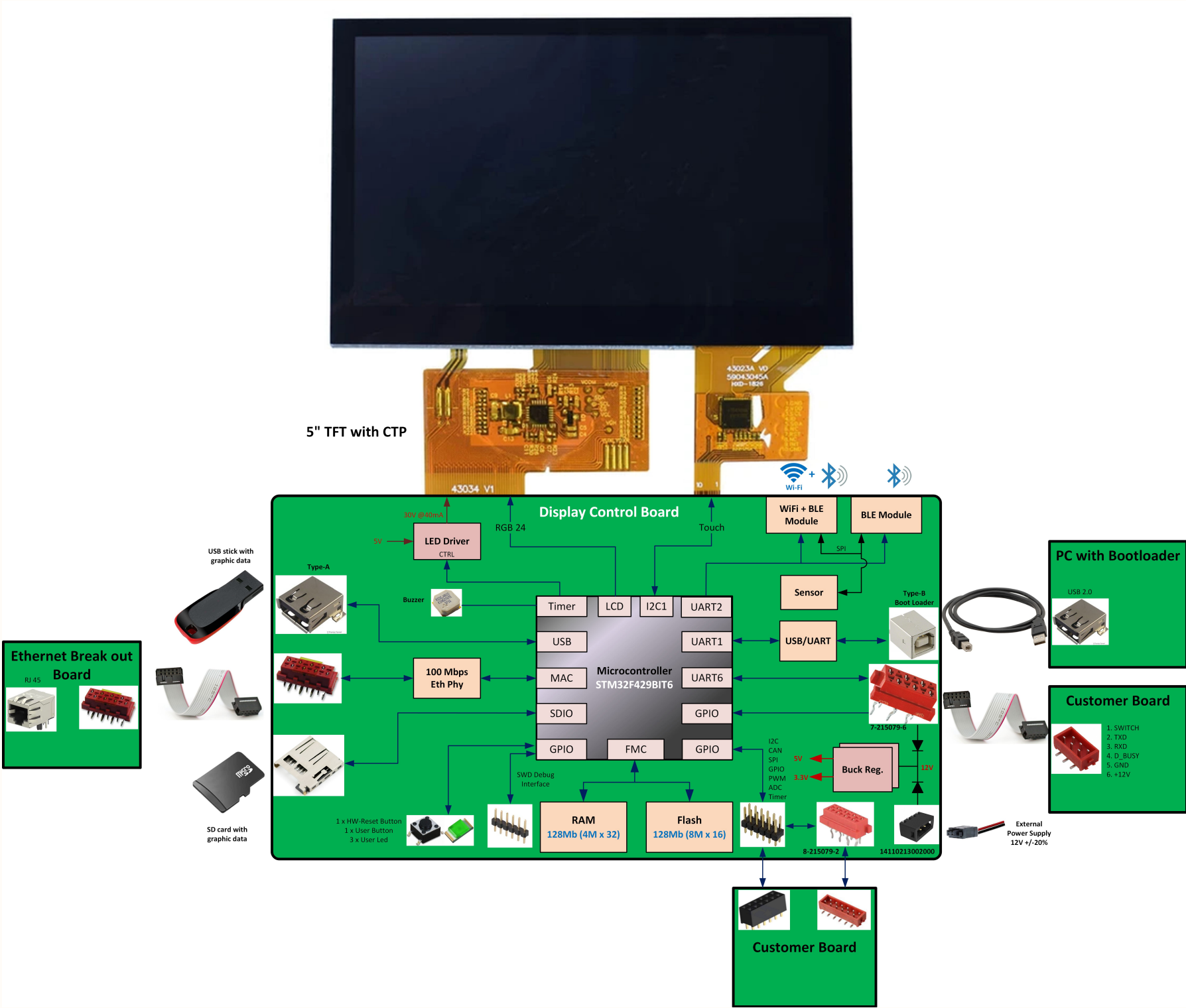
DS18_SYSG_DISP_1116

DISPLAY CONTROL BOARD 5 INCH

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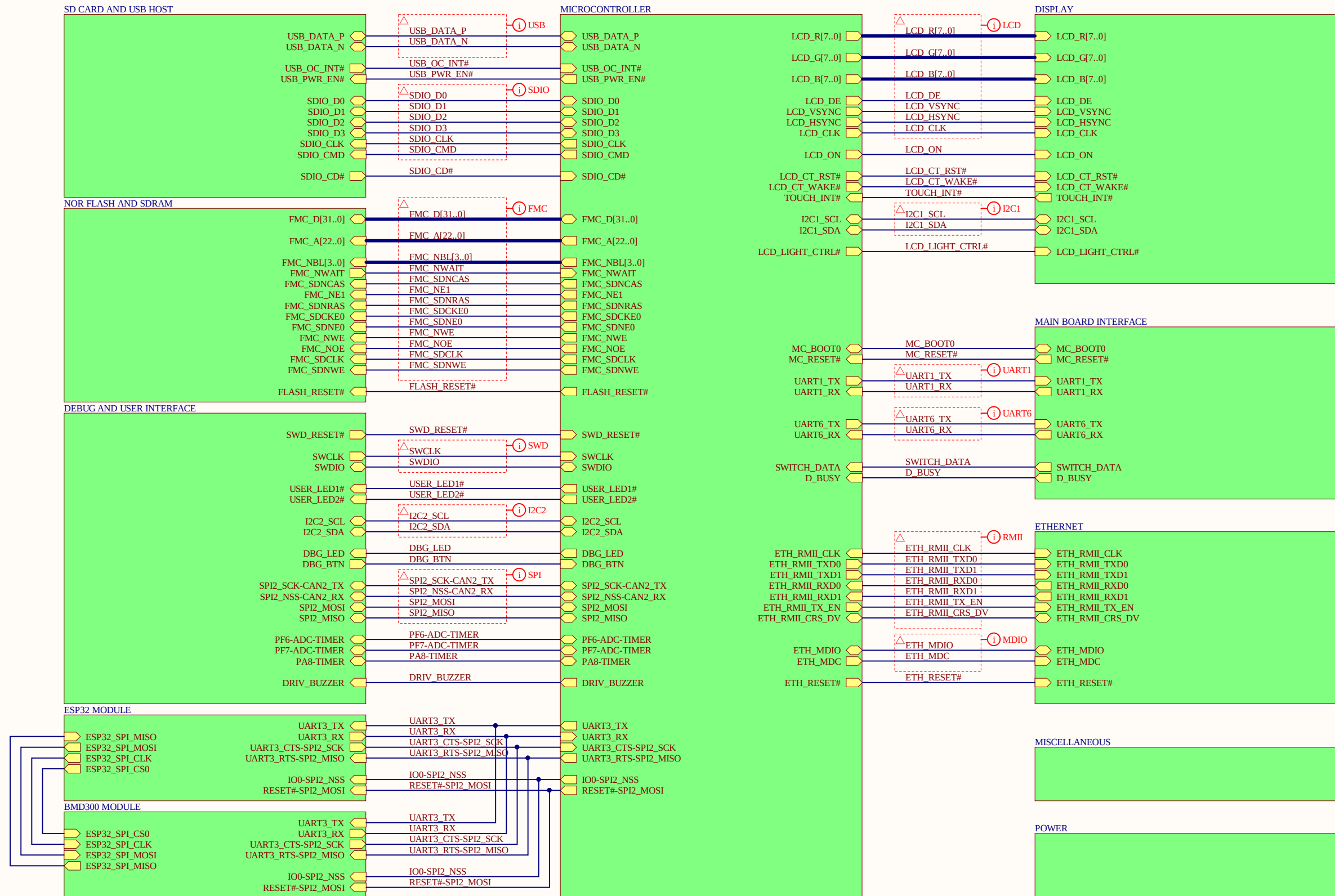
Schematics			
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P01_COVER_PAGE.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	1

BLOCK DIAGRAM



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P02_Block_Diagram.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	2

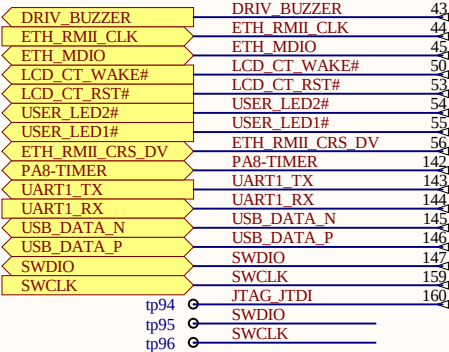
TOP LEVEL PAGE



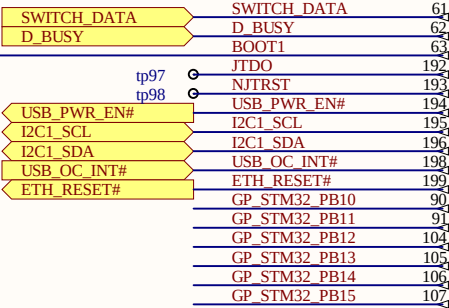
Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P03_TOP_LEVEL_PAGE.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	3

MICROCONTROLLER A-B

Boot mode selection pins		Boot mode
BOOT1	BOOT0	
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM

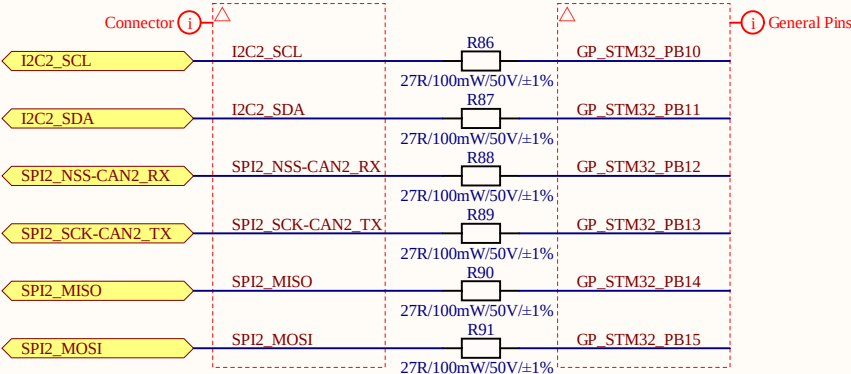


IC1A STM32F429BIT6
PA0/TIM2_CH1/TIM2_ETR/TIM5_CH1/TIM8_ETR/USART2_CTS/UART4_TX/ETH_MII_CRD_EVENTOUT/ADC123_IN0/WKUP
PA1/TIM2_CH2/TIM5_CH2/USART2_RTS/UART4_RX/ETH_MII_RX_CLK/ETH_RMII_REF_CLK_EVENTOUT/ADC123_IN1
PA2/TIM2_CH3/TIM5_CH3/TIM9_CH1/USART2_TX/ETH_MDIO_EVENTOUT/ADC123_IN2
PA3/TIM2_CH4/TIM5_CH4/TIM9_CH2/USART2_RX/OTG_HS_ULPI_D0/ETH_MII_COL/LCD_B5_EVENTOUT/ADC123_IN3
PA4/SPI1_NSS/SPI3_NSS/I2S3_WS/USART2_CK/OTG_HS_SOF/DCML_HSYNC/LCD_VSYNC_EVENTOUT/ADC12_IN4/DAC_OUT1
PA5/TIM2_CH1/TIM2_ETR/TIM8_CH1N/SPI1_SCK/OTG_HS_ULPI_CK_EVENTOUT/ADC12_IN5/DAC_OUT2
PA6/TIM1_BKIN/TIM3_CH1/TIM8_BKIN/SPI1_MISO/TIM13_CH1/DCML_PIXCLK/LCD_G2_EVENTOUT/ADC12_IN6
PA7/TIM1_CH1N/TIM3_CH2/TIM8_CH1N/SPI1_MOSI/TIM14_CH1/ETH_MII_RX_DV/ETH_RMII_CRD_DV_EVENTOUT/ADC12_IN7
PA8/MCO1/TIM1_CH1/I2C3_SCL/USART1_CK/OTG_FS_SOF/LCD_R6_EVENTOUT
PA9/TIM1_CH2/I2C3_SMBA/USART1_TX/DCML_D0_EVENTOUT/OTG_FS_VBUS
PA10/TIM1_CH3/USART1_RX/OTG_FS_ID/DCML_D1_EVENTOUT
PA11/TIM1_CH4/USART1_CTS/CAN1_RX/LCD_R4/OTG_FS_DM_EVENTOUT
PA12/TIM1_ETR/USART1_RTS/CAN1_TX/LCD_R5/OTG_FS_DP_EVENTOUT
PA13/JTMS-SWDIO_EVENTOUT
PA14/JTCK-SWCLK_EVENTOUT
PA15/JTDI/TIM2_CH1/TIM2_ETR/SPI1_NSS/SPI3_NSS/I2S3_WS_EVENTOUT



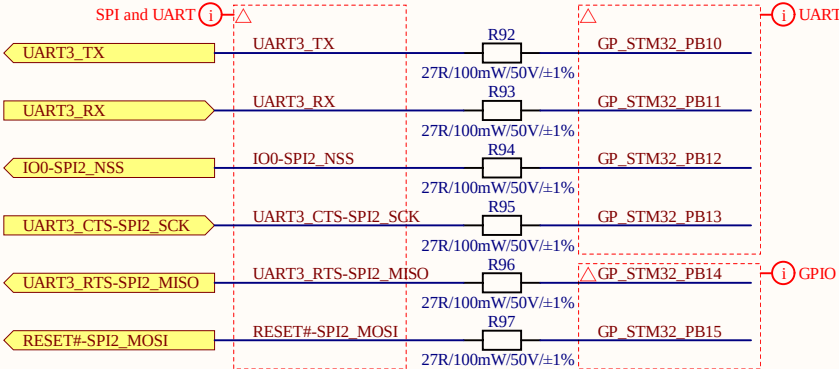
IC1B STM32F429BIT6
PB0/TIM1_CH2N/TIM3_CH3/TIM8_CH2N/LCD_R3/OTG_HS_ULPI_D1/ETH_MII_RXD2_EVENTOUT/ADC12_IN8
PB1/TIM1_CH3N/TIM3_CH4/TIM8_CH3N/LCD_R6/OTG_HS_ULPI_D2/ETH_MII_RXD3_EVENTOUT/ADC12_IN9
PB2_EVENTOUT/BOOT1
PB3/JTDO/TRACESWO/TIM2_CH2/SPI1_SCK/SPI3_SCK/I2S3_CK_EVENTOUT
PB4/NJTRST/TIM3_CH1/SPI1_MISO/SPI3_MISO/I2S3ext_SD_EVENTOUT
PB5/TIM3_CH2/I2C1_SMBA/SPI1_MOSI/SPI3_MOSI/I2S3_SD/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/FMC_SDCKE1/DCML_D10_EVENTOUT
PB6/TIM4_CH1/I2C1_SCL/USART1_TX/CAN2_TX/FMC_SDNE1/DCML_D5_EVENTOUT
PB7/TIM4_CH2/I2C1_SDA/USART1_RX/FMC_NL/DCML_VSYNC_EVENTOUT
PB8/TIM4_CH3/TIM10_CH1/I2C1_SCL/CAN1_RX/ETH_MII_TXD3/SDIO_D4/DCML_D6/LCD_B6_EVENTOUT
PB9/TIM4_CH4/TIM11_CH1/I2C1_SDA/SPI2_NSS/I2S2_WS/CAN1_TX/SDIO_D5/DCML_D7/LCD_B7_EVENTOUT
PB10/TIM2_CH3/I2C2_SCL/SPI2_SCK/I2S2_CK/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/LCD_G4_EVENTOUT
PB11/TIM2_CH4/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_MII_TX_EN/ETH_RMII_TX_EN/LCD_G5_EVENTOUT
PB12/TIM1_BKIN/I2C2_SMBA/SPI2_NSS/I2S2_WS/USART3_CK/CAN2_RX/OTG_HS_ULPI_D5/ETH_MII_TXD0/ETH_RMII_TXD0/OTG_HS_ID_EVENTOUT
PB13/TIM1_CH1N/SPI2_SCK/I2S2_CK/USART3_CTS/CAN2_TX/OTG_HS_ULPI_D6/ETH_MII_TXD1/ETH_RMII_TXD1_EVENTOUT/OTG_HS_VBUS
PB14/TIM1_CH2N/TIM8_CH2N/SPI2_MISO/I2S2ext_SD/USART3_RTS/TIM12_CH1/OTG_HS_DM_EVENTOUT
PB15/RTC_REFIN/TIM1_CH3N/TIM8_CH3N/SPI2_MOSI/I2S2_SD/TIM12_CH2/OTG_HS_DP_EVENTOUT

External Connector Connection



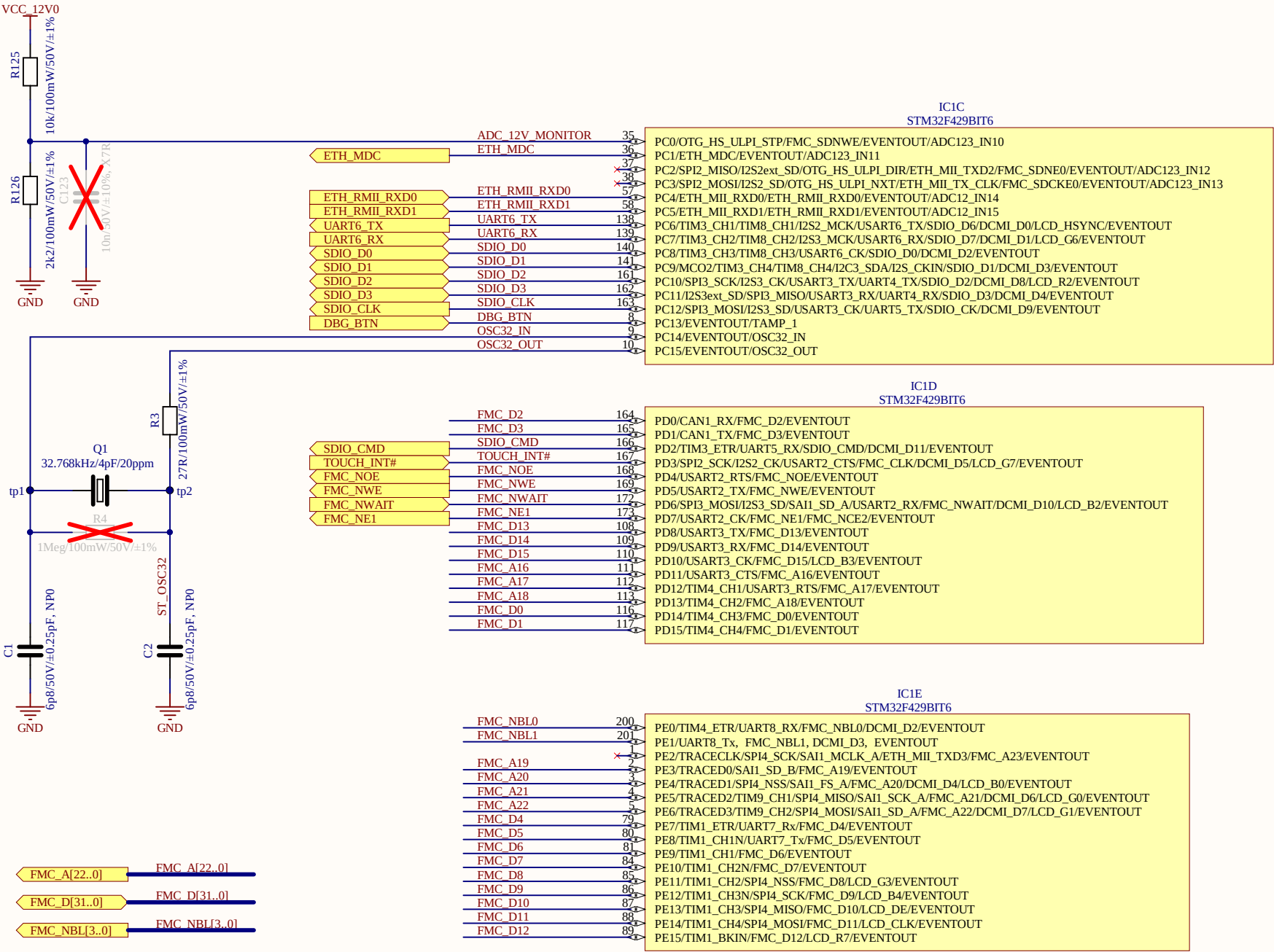
Mount R86 to R91 : STM32 Interfaces available on X10 and X11
Mount R92 to R97 : UART/SPI Interface for Module/Sensor
Don't populate both group at the same time.

Sensor / wireless module Connection



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb	www.ebs-systart.com	
Document:	P04_Microcontroller_A-B.SchDoc	Date:	20-Apr-2020
Author:	DCT/VKN	Date:	27-Apr-2020
Auditor:	DCT/AVR	Page:	4
Status:	Approved		

MICROCONTROLLER C-E



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb		
Document:	P05_Microcontroller_C-E.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	5

MICROCONTROLLER F-K

A

B

C

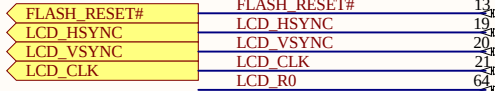
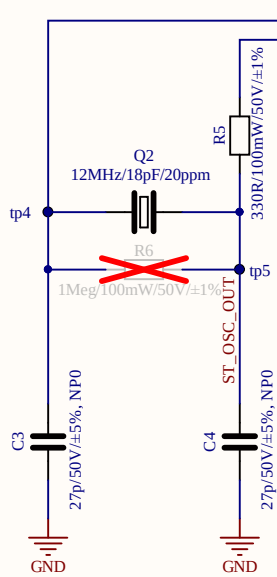
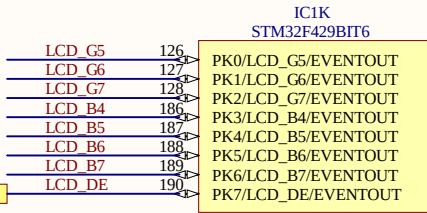
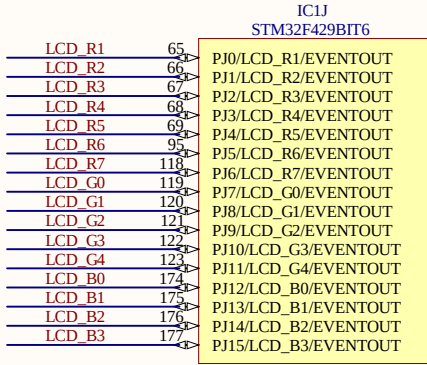
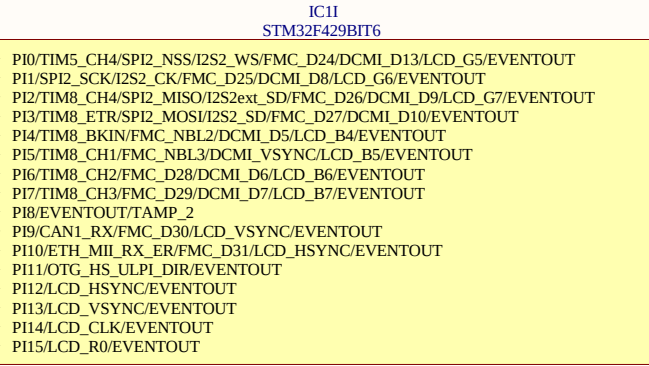
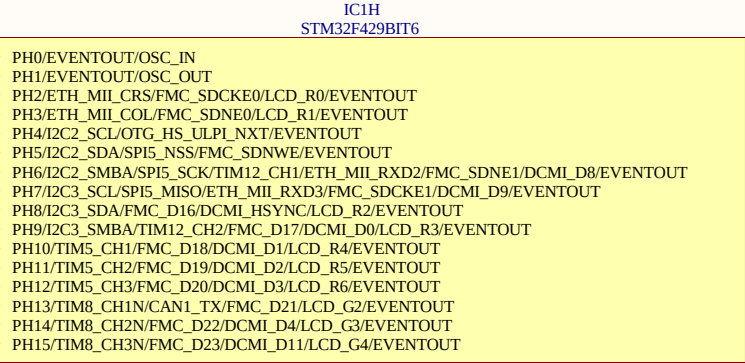
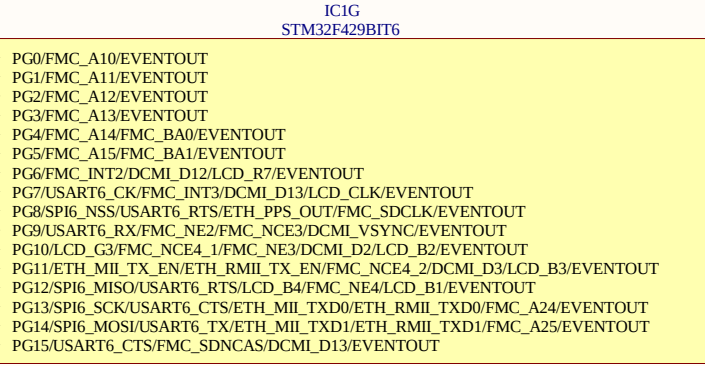
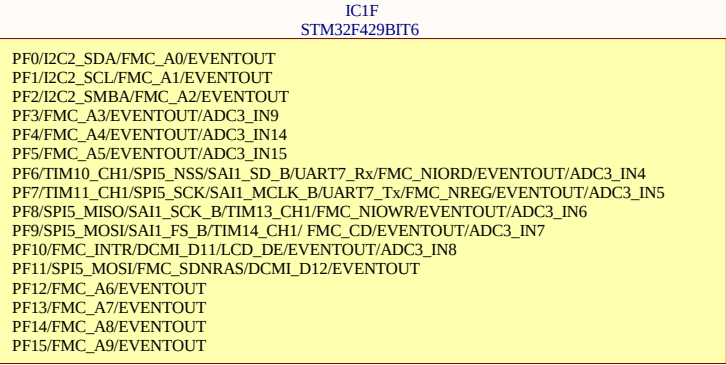
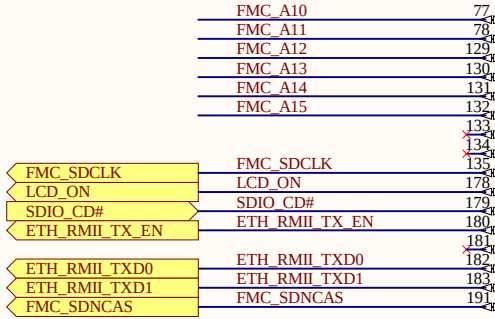
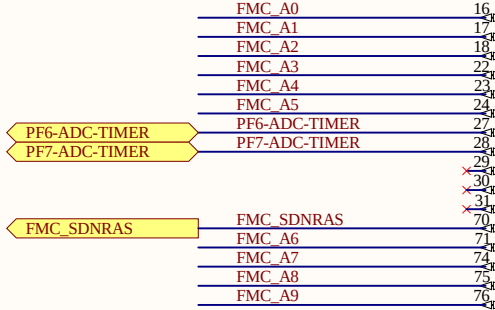
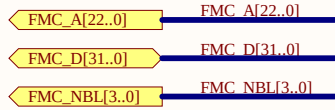
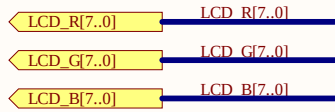
D

A

B

C

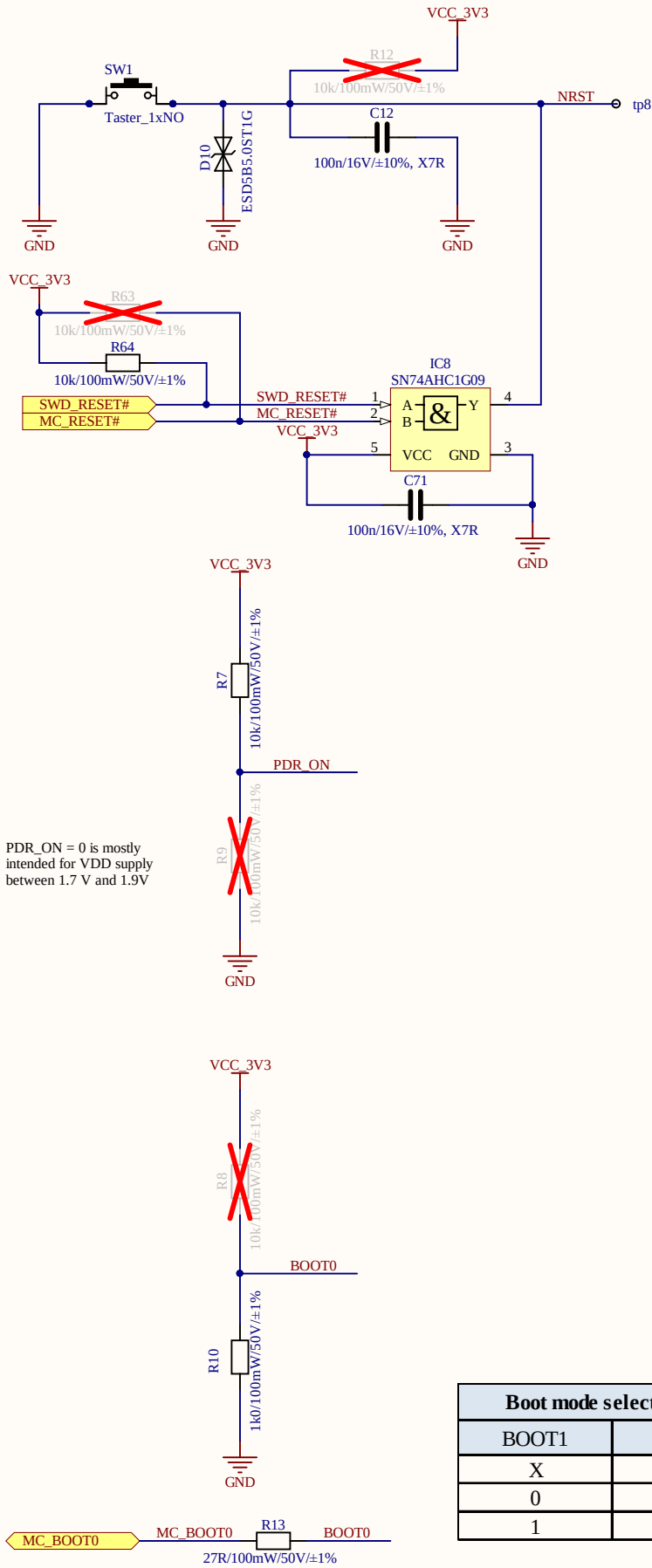
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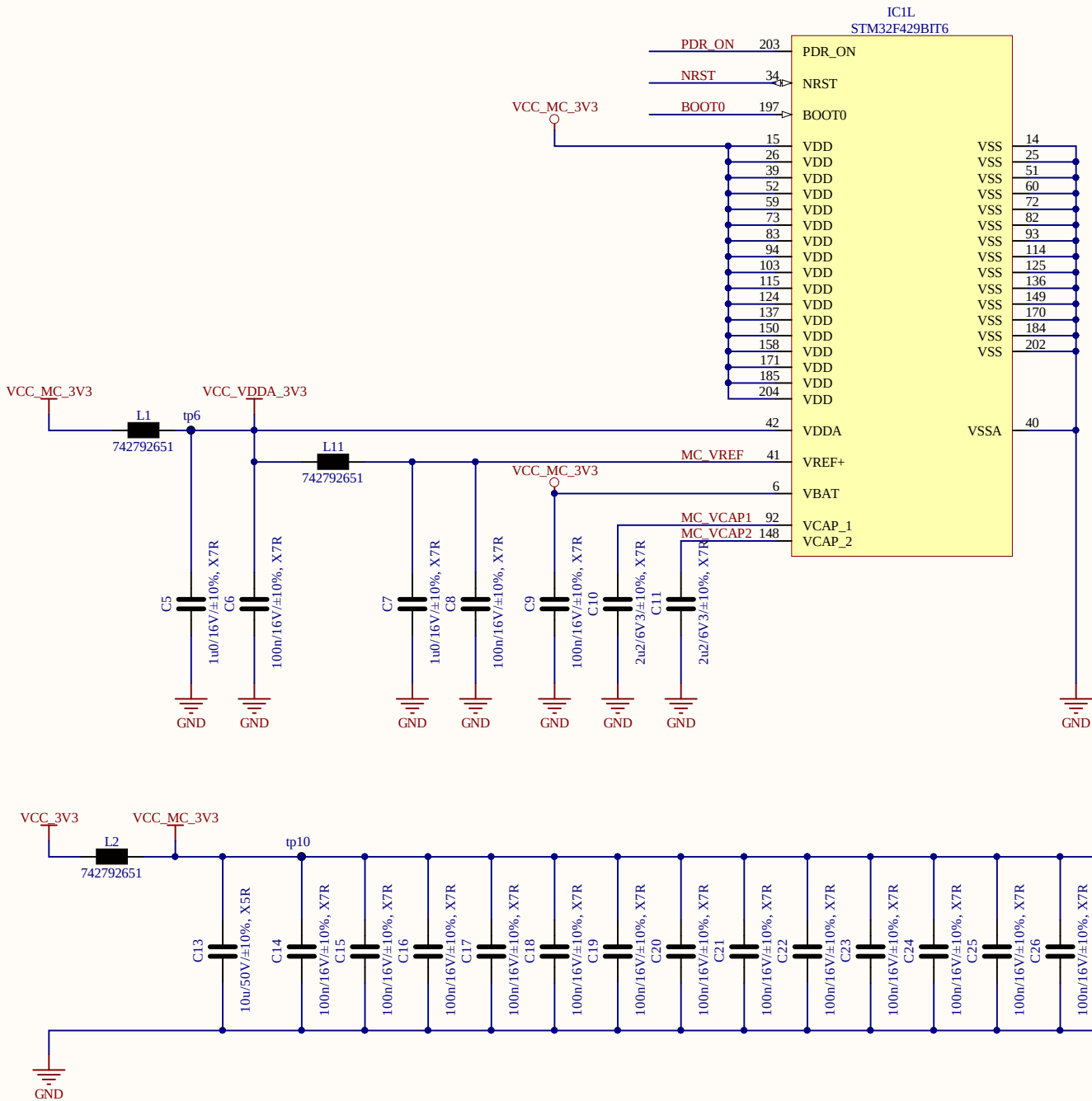
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrijPcb		
Document:	P06_Microcontroller_F-K.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	6

MICROCONTROLLER POWER

MicroController Reset



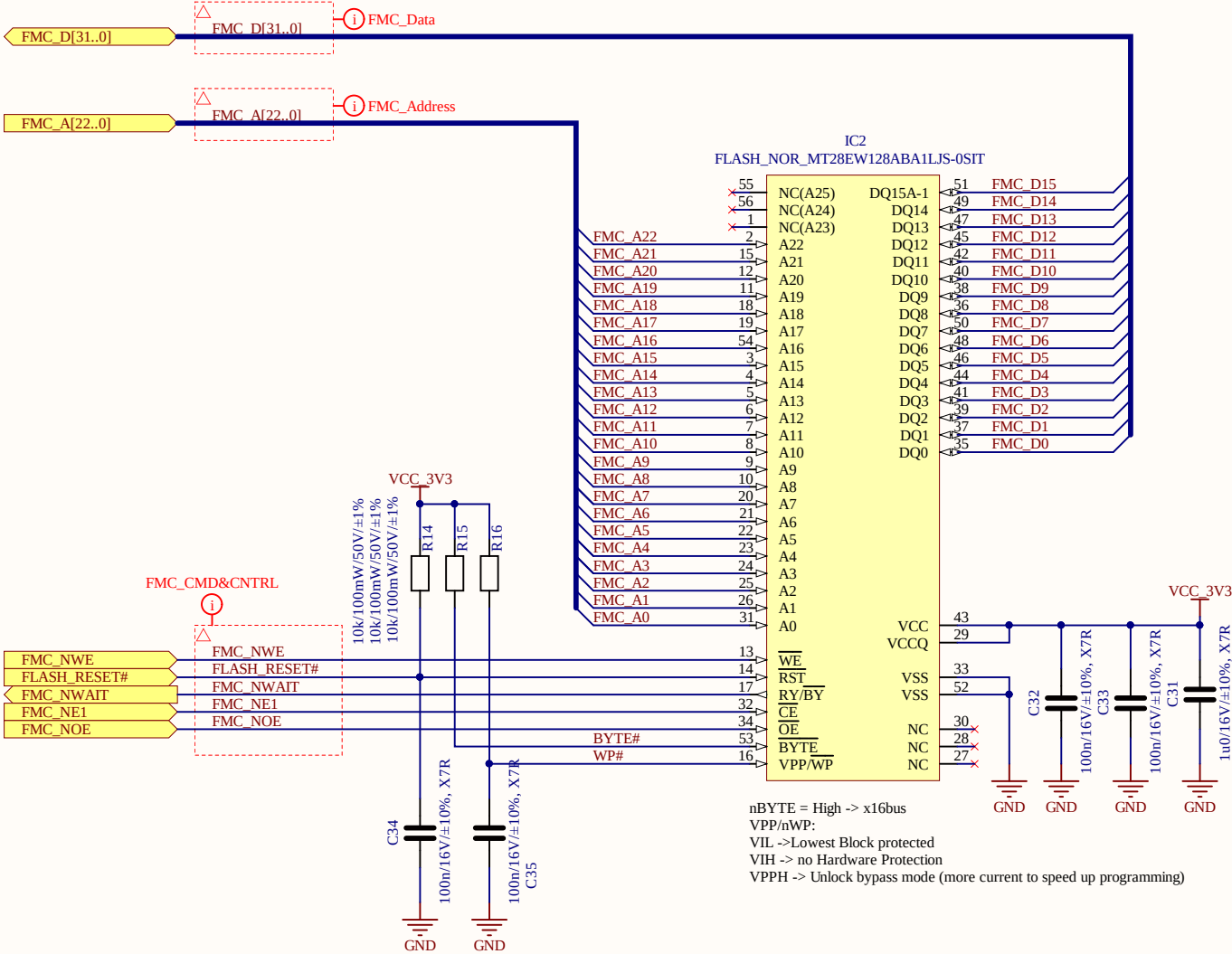
Boot mode selection pins		Boot mode
BOOT1	BOOT0	
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM



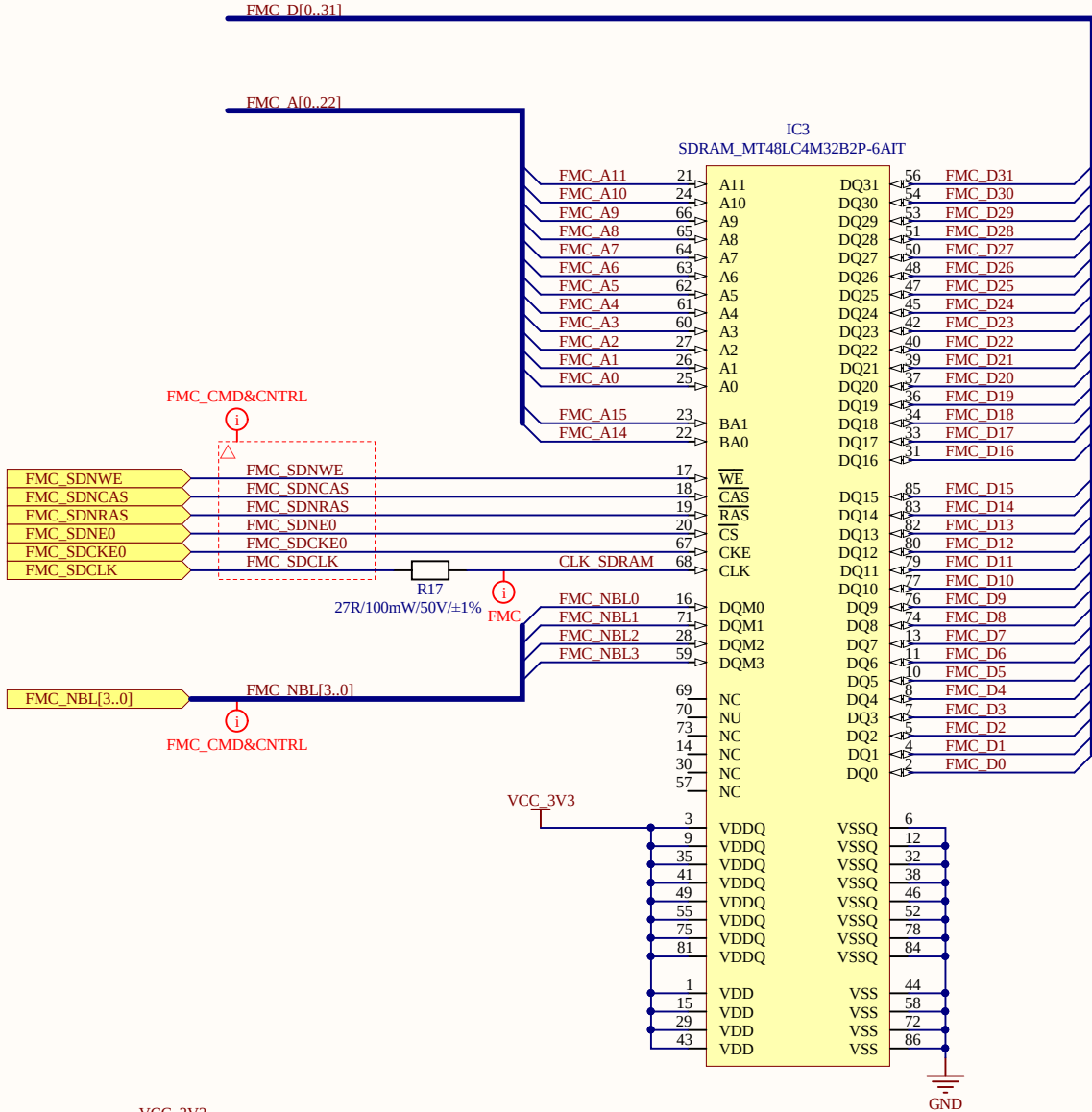
Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P07_Microcontroller_Power.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	7

NOR FLASH AND SDRAM

NOR FLASH

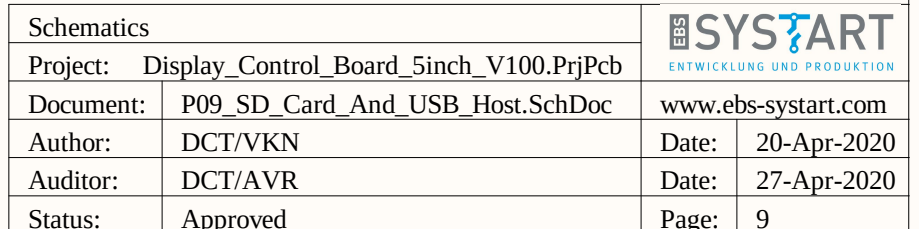


SDRAM



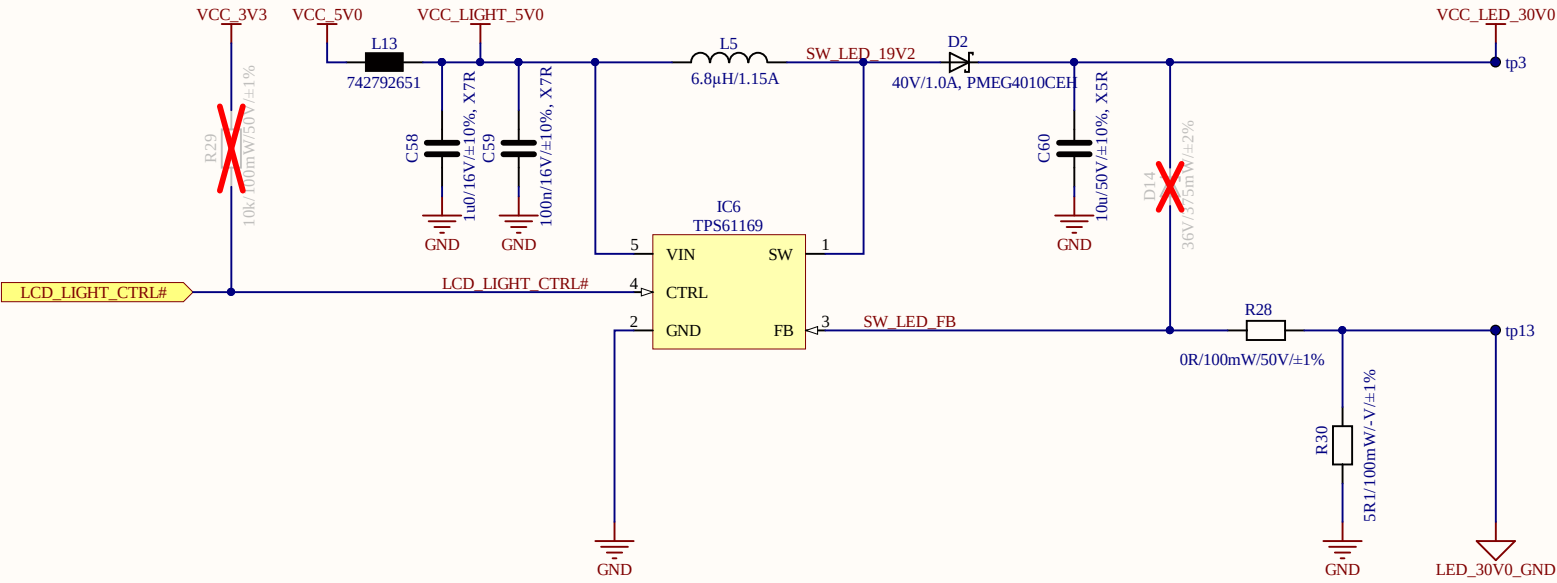
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb		
Document:	P08_NOR_Flash_and_SDRAM.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	8

MICRO SD CARD INTERFACE

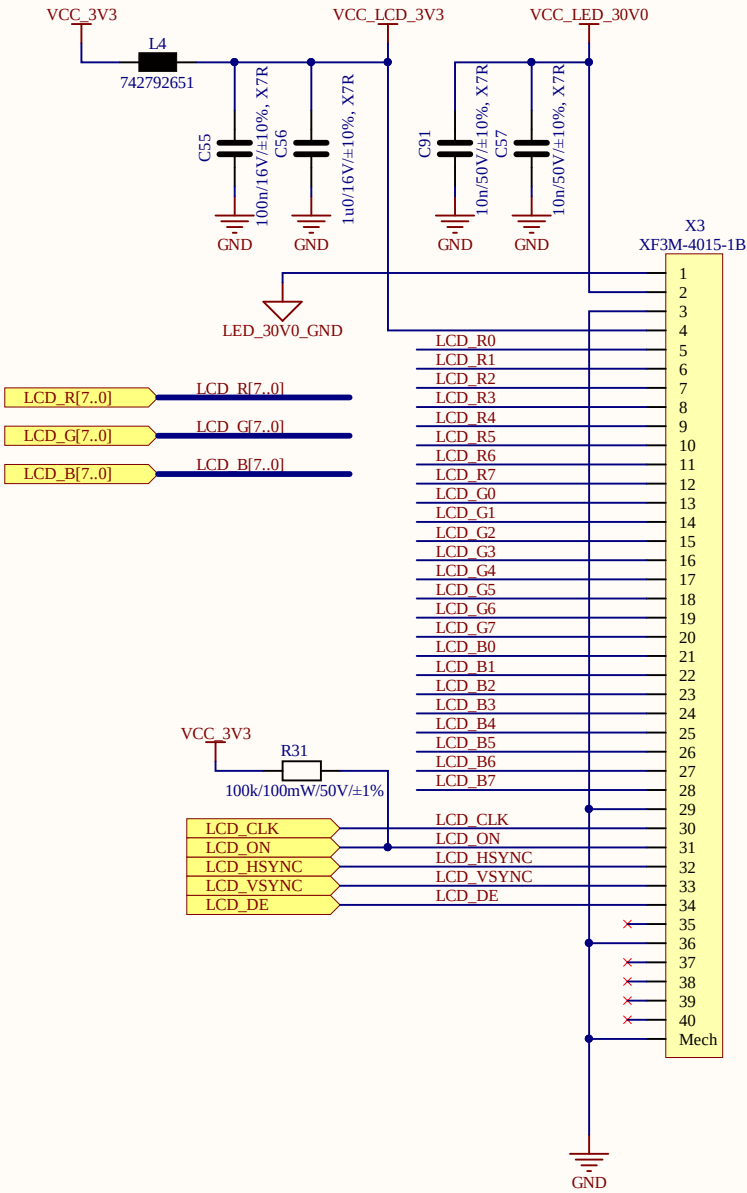


TFT DISPLAY

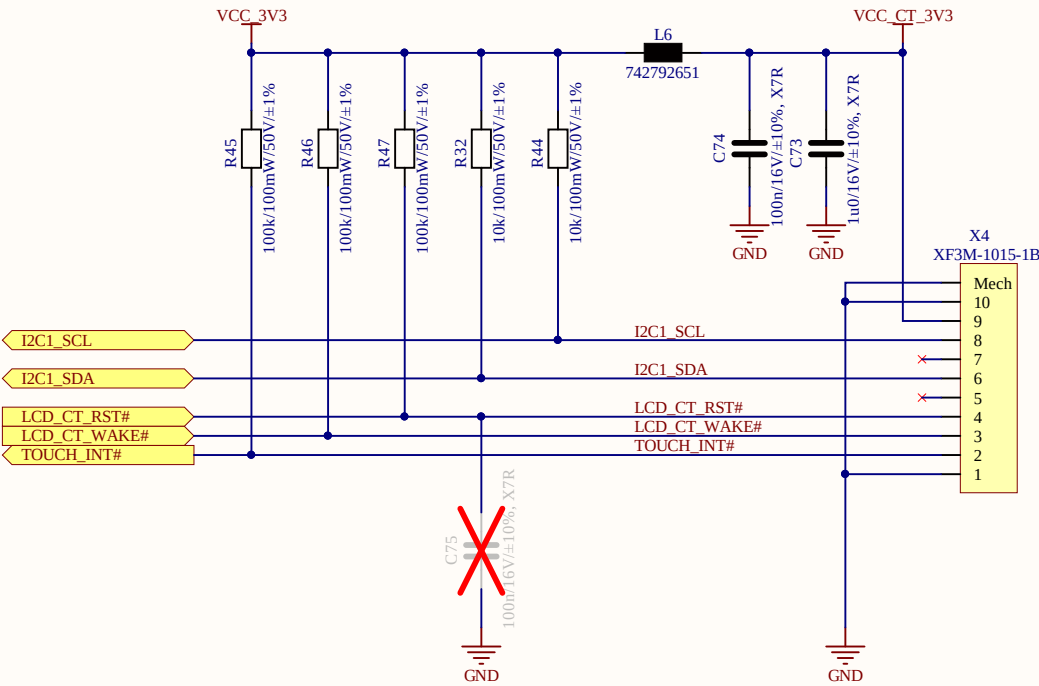
LCD Back Light



Display Connector

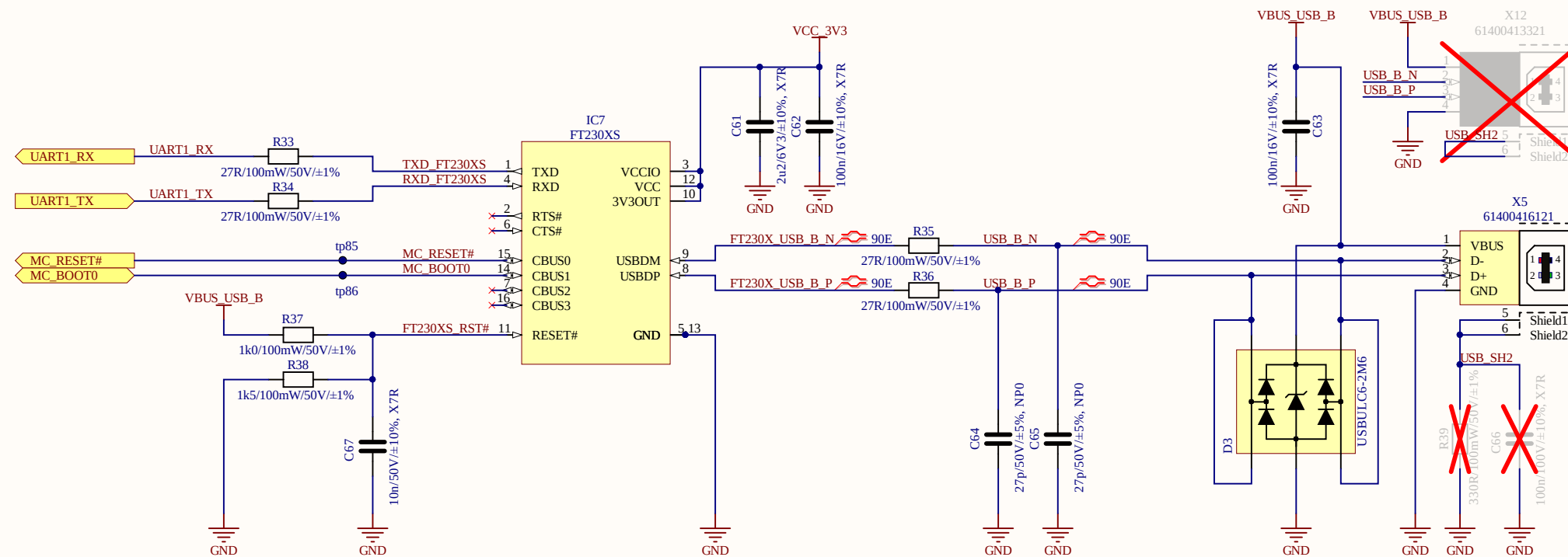


Touch Panel Connector



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrfPcb	www.ebs-systart.com	
Document:	P10_TFT_Display.SchDoc	Date:	20-Apr-2020
Author:	DCT/VKN	Date:	27-Apr-2020
Auditor:	DCT/AVR	Page:	10
Status:	Approved		

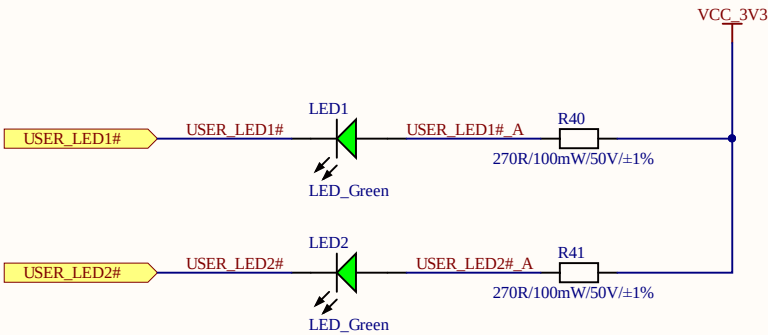
USB Type B Inetrface



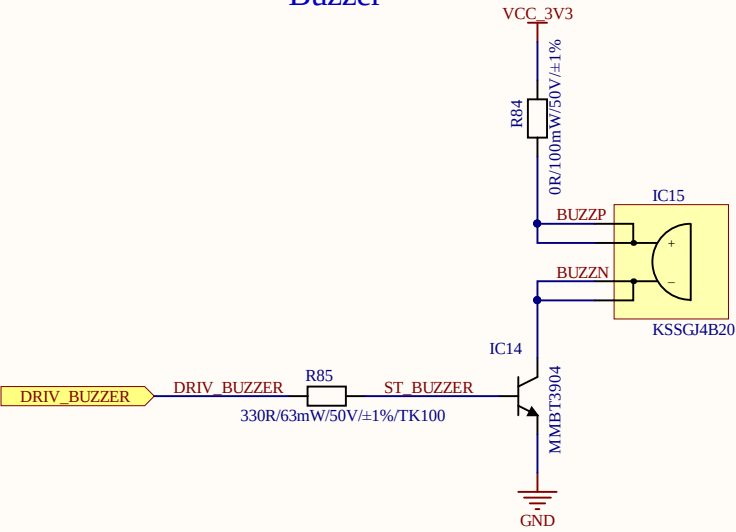
Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P11_Main_Board_Interface.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	11

DEBUG AND USER INTERFACE

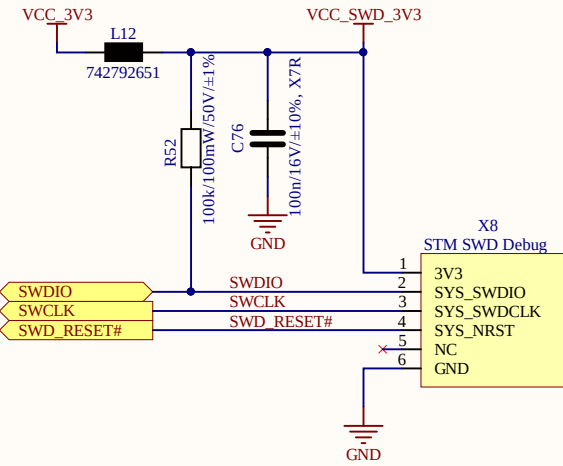
User Interface LED



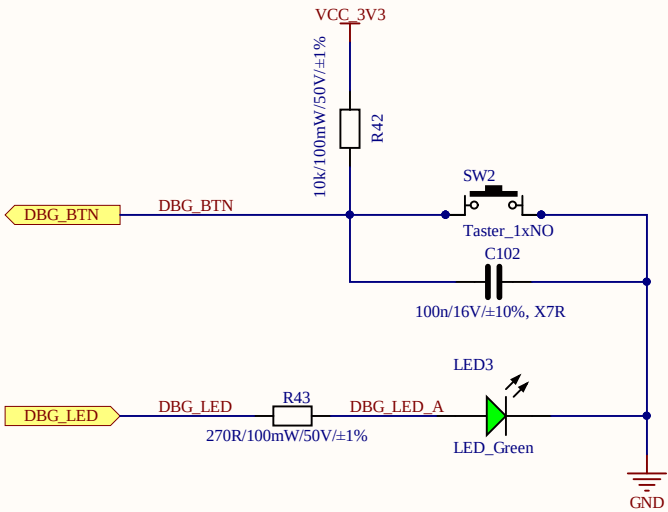
Buzzer



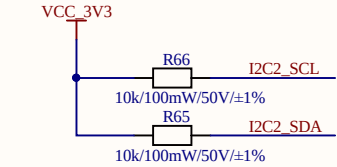
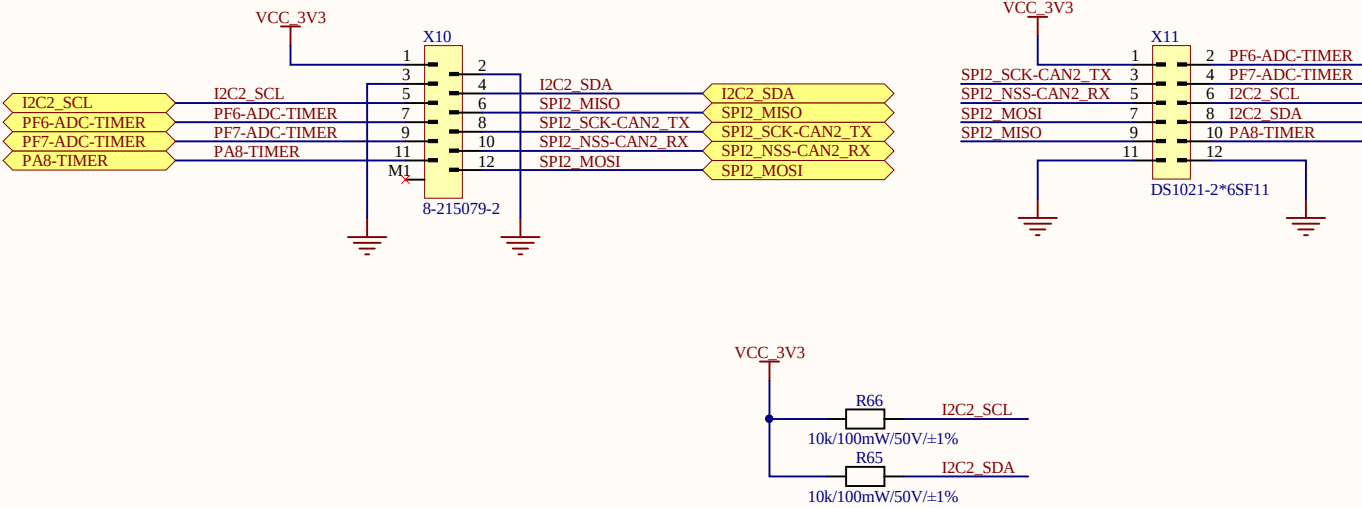
Serial wire Debug Port



Debug Interface

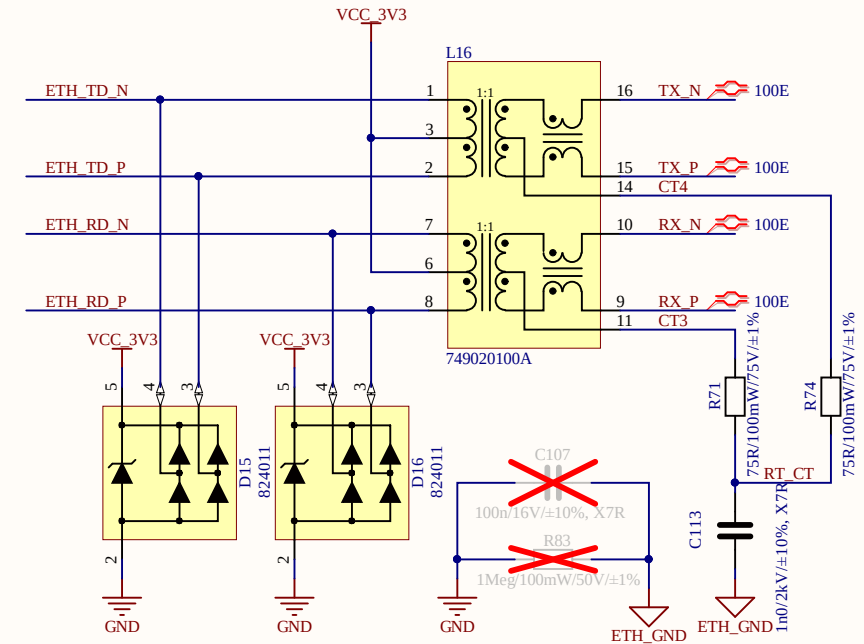
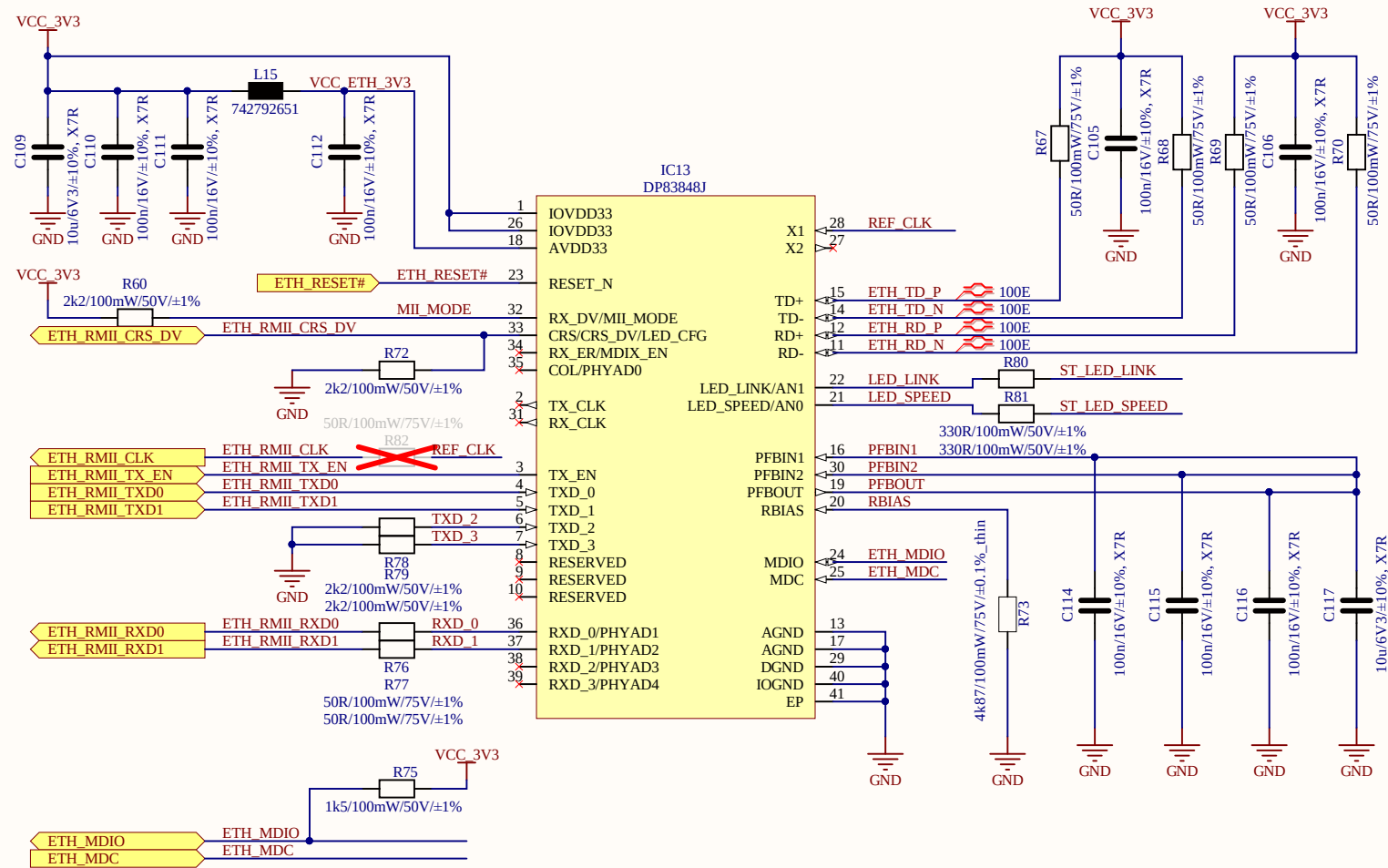


External Interface

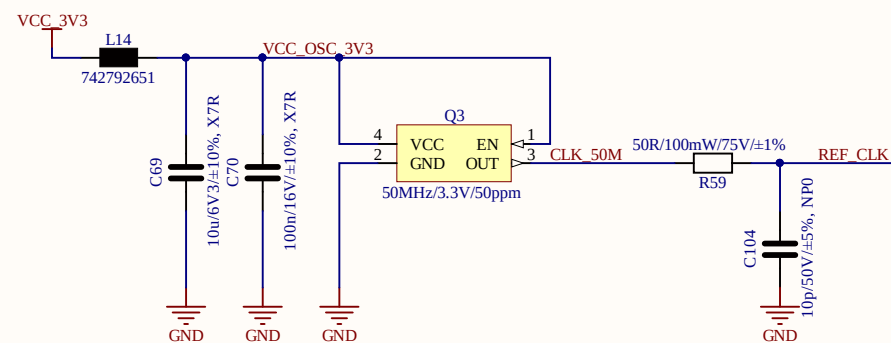


Schematics		 ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb		
Document:	P12_Debug_And_User_Interface.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	12

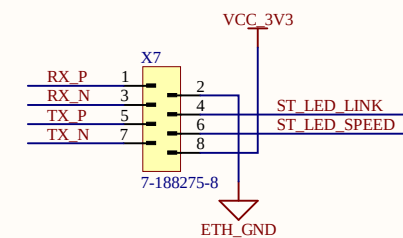
ETHERNET INTERFACE



OSCILLATOR



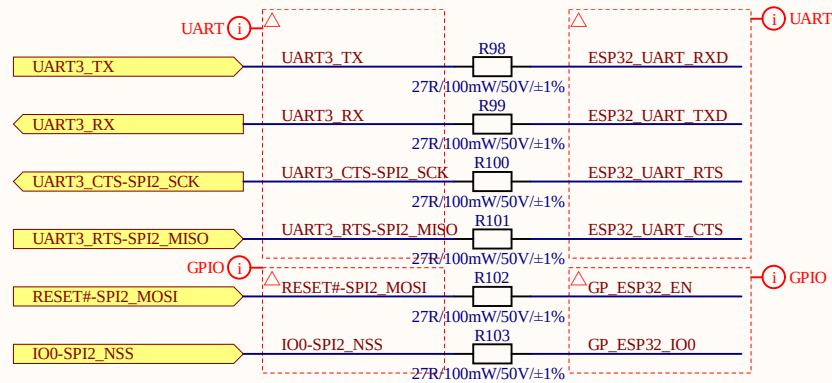
ETHERNET CONNECTOR



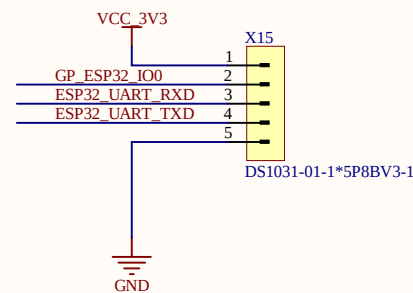
Schematics		 ENTWICKLUNG UND PRODUKTION			
Project: Display_Control_Board_5inch_V100.PrjPcb					
Document:	P13_Ethernet_Interface.SchDoc			www.ebs-systart.com	
Author:	DCT/VKN			Date:	20-Apr-2020
Auditor:	DCT/AVR			Date:	27-Apr-2020
Status:	Approved			Page:	13

ESP32 Module

Mount R98 to R103 : STM32 to ESP32 UART Interface available
Mount R107 to R112 : STM32 to BMD300 UART Interface available
STM32 UART Interface will not available to both module at the same

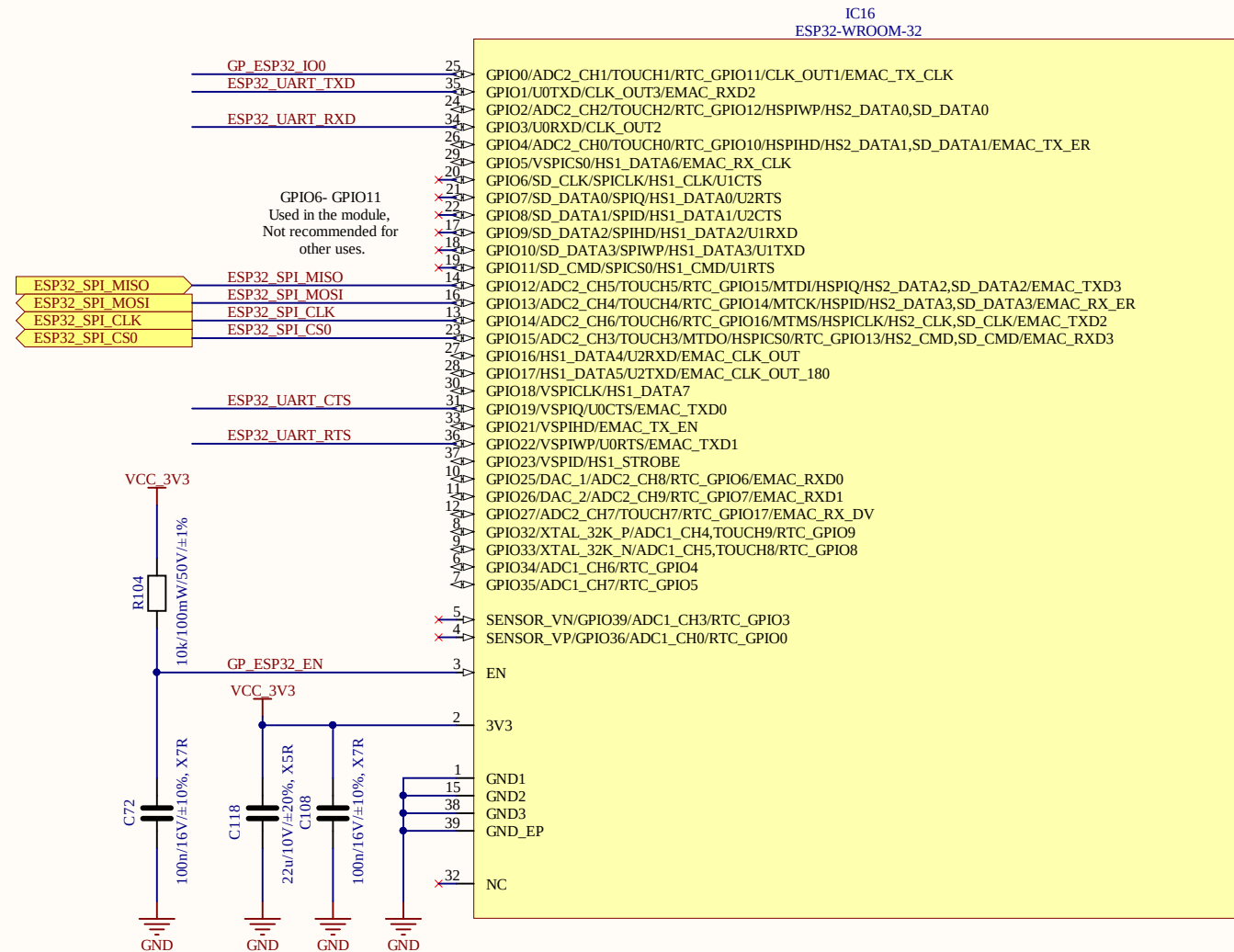


UART DOWNLOAD



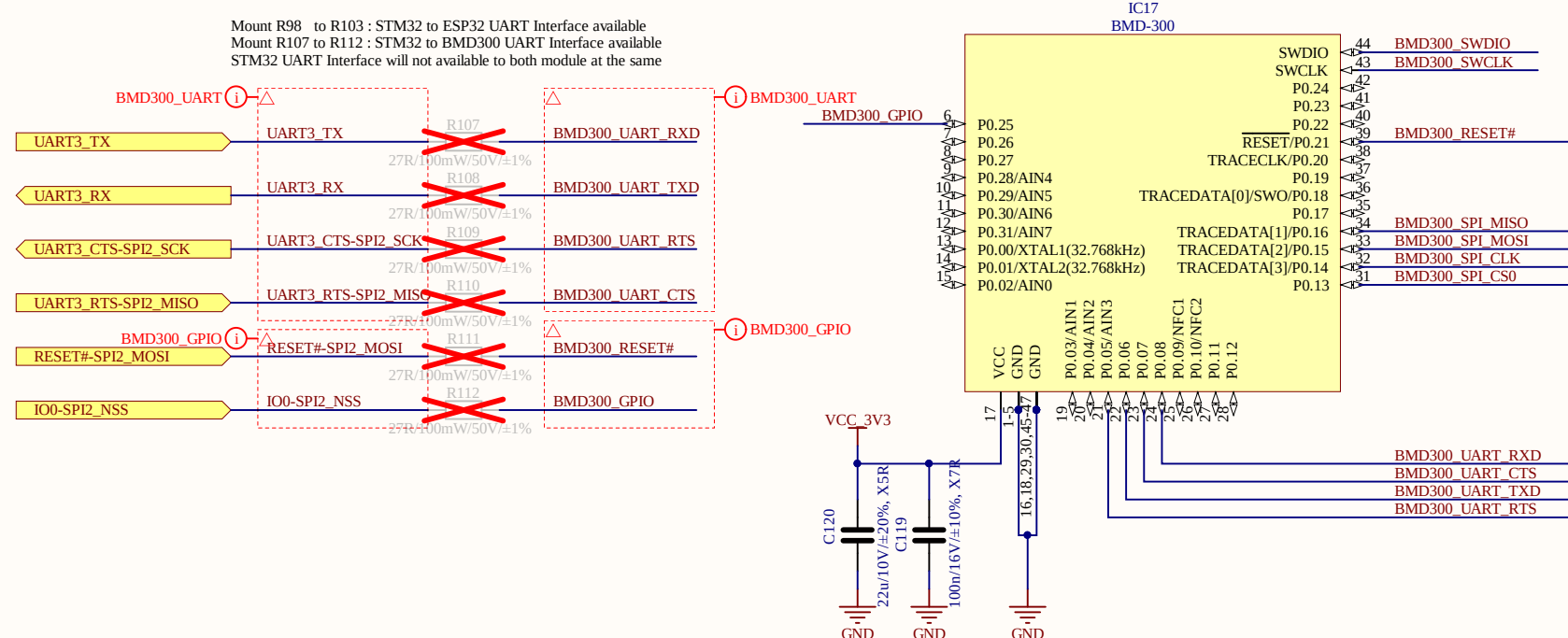
GPIO0	GPIO2	Booting Mode
1 (Default)	x	SPI Boot (Default)
0	0 (Default)	Download Boot

Pin	Value	Configuration
MTDI (GPIO12)	0(Default)	Voltage of Internal LDO = 3.3
	1	Voltage of Internal LDO = 1.8
MTDO (GPIO15)	0	U0TXD Silent
	1(Default)	U0TXD Active

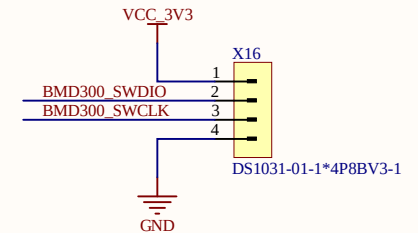


Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P14_ESP32_Module.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	14

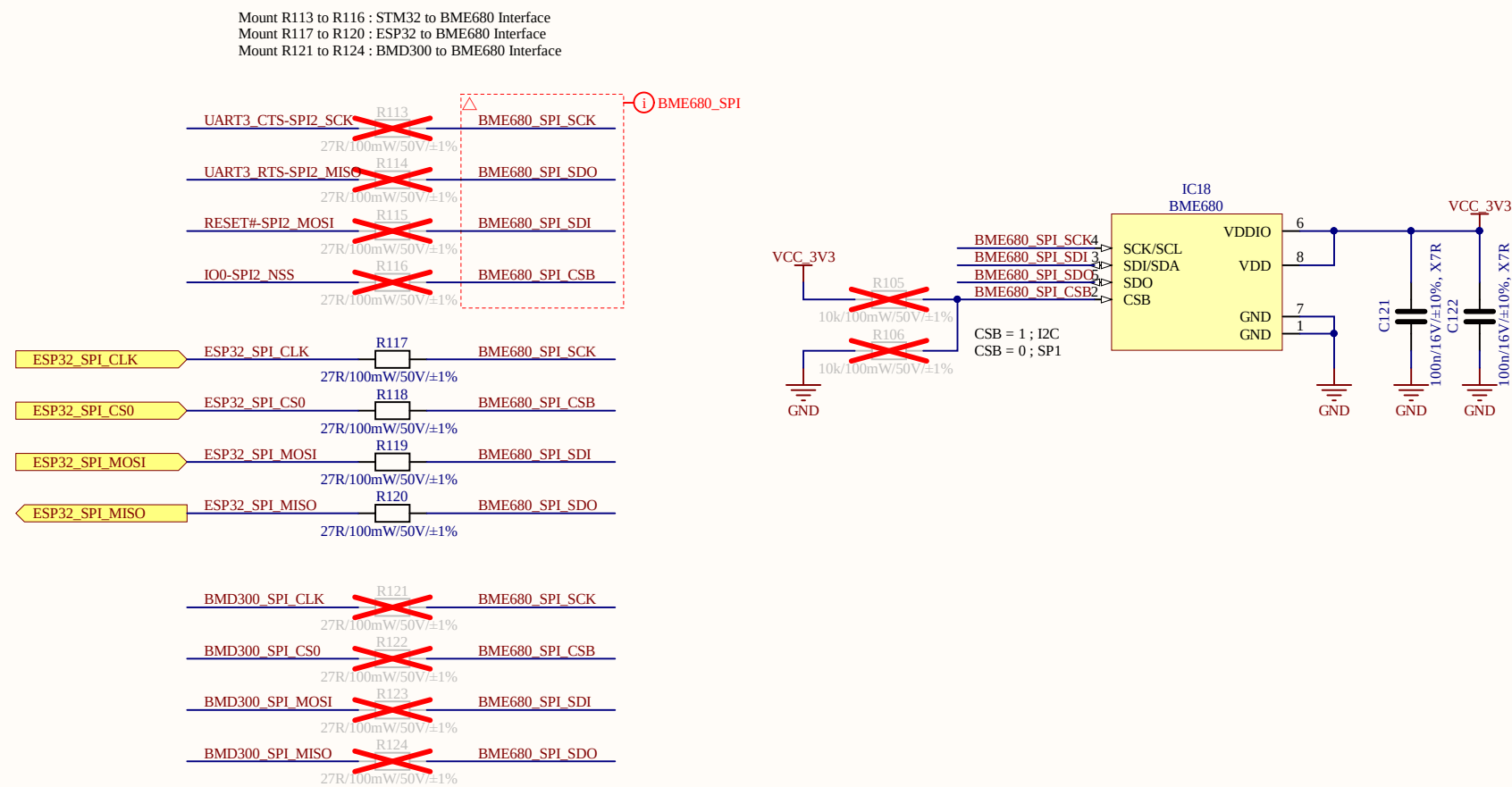
BMD 300 MODULE



BMD300 SWD HEADER

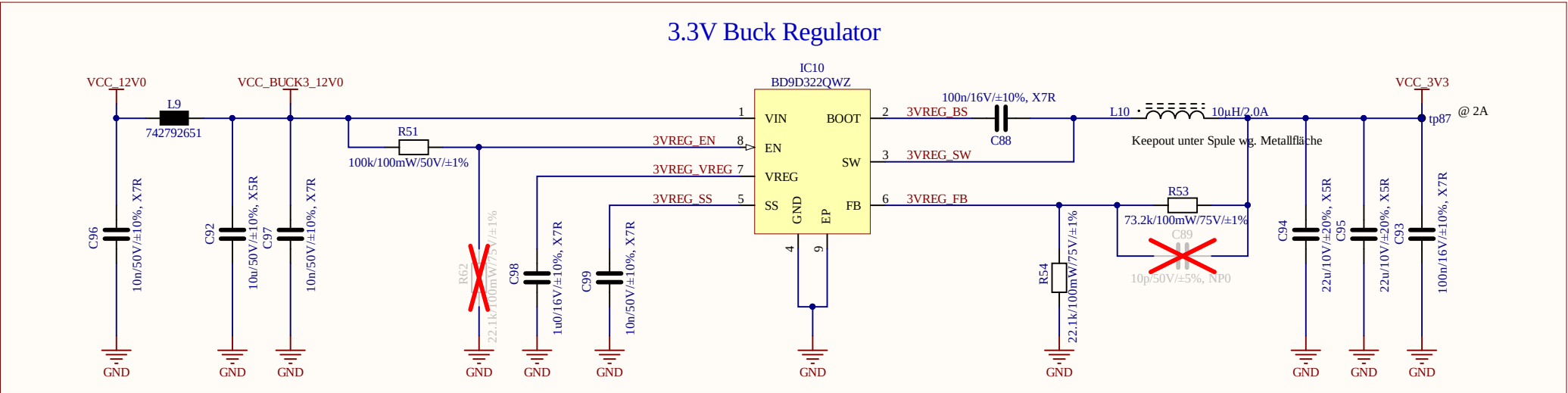
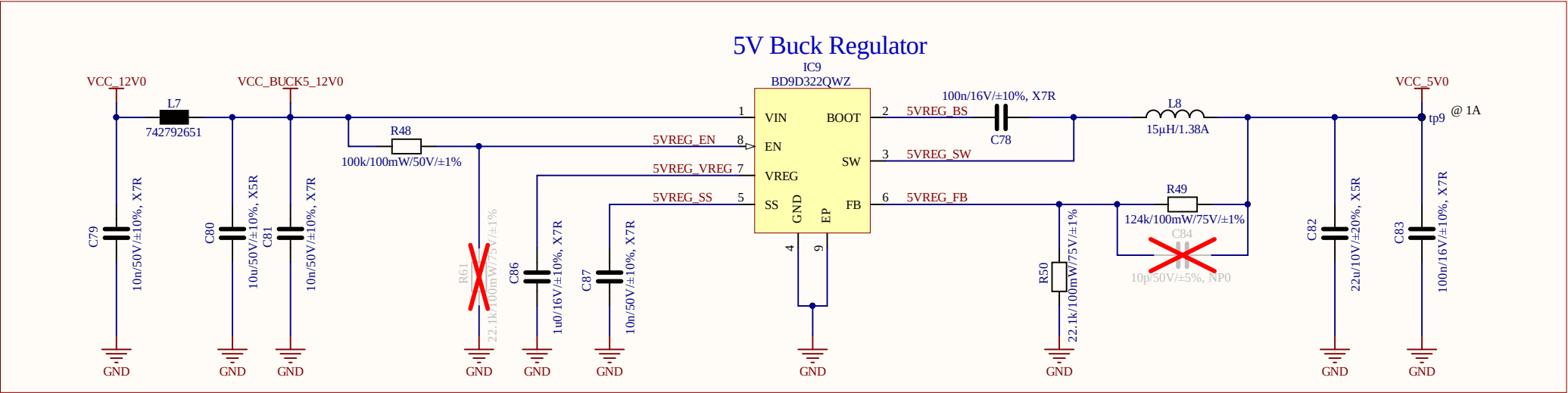
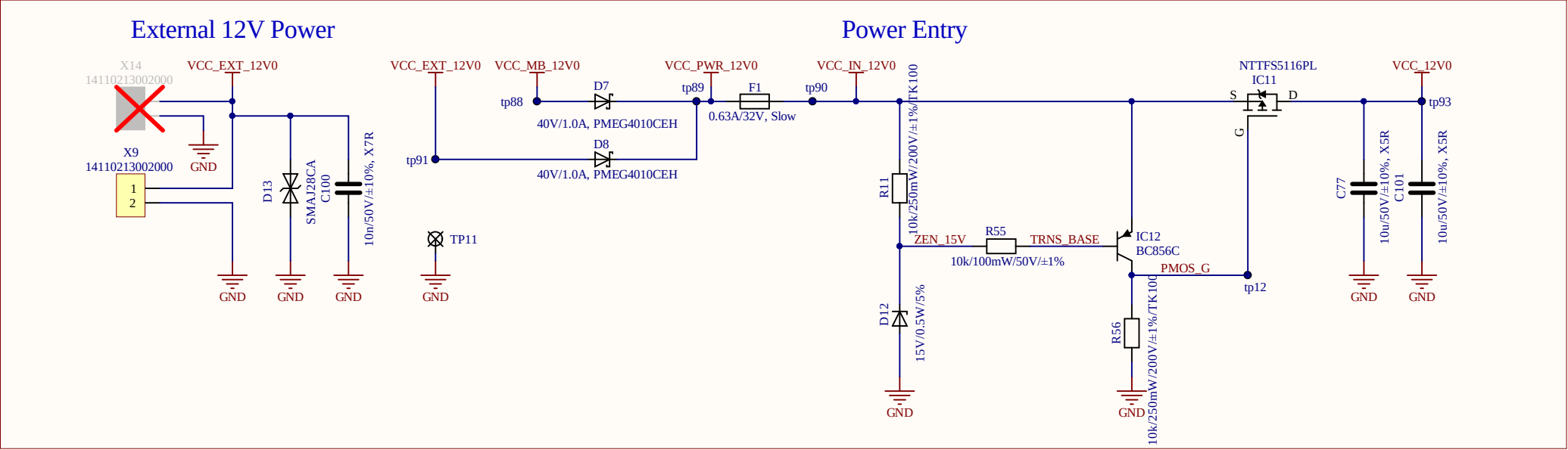


BME680 SENSOR



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_5inch_V100.PrjPcb			
Document:	P15_BMD300_Module.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	15

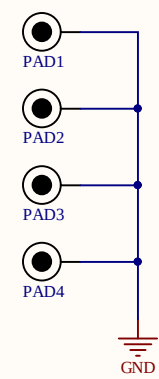
POWER



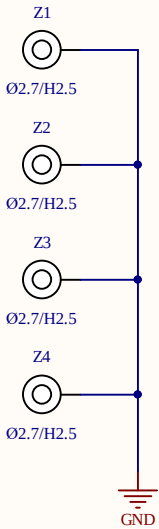
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb		
Document:	P16_Power.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	16

MISCELLANEOUS

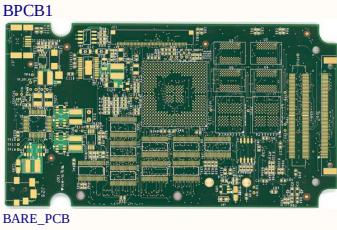
MOUNTING HOLES



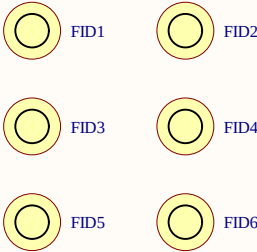
STEEL SPACER



BARE PCB



FIDUCIALS



Schematics		 ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_5inch_V100.PrjPcb		
Document:	P17_Miscellaneous.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	20-Apr-2020
Auditor:	DCT/AVR	Date:	27-Apr-2020
Status:	Approved	Page:	17

